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TITLE: Method and apparatus for handling invalidation requests to processors not present in a computer system  
  
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PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>5394555</u>	February 1995	Hunter et al.	711/148
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<input type="checkbox"/>	<u>5802578</u>	September 1998	Lovett	711/147
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<input type="checkbox"/>	<u>6092155</u>	July 2000	Olnowich	711/142

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ART-UNIT: 2183

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## ABSTRACT:

A node controller (12) in a computer system (10) includes a processor interface unit (24), a memory directory interface unit (22), and a local block unit (28). In response to a memory location in a memory (17) associated with the memory directory interface unit (22) being altered, the processor interface unit (24) generates an invalidation request for transfer to the memory directory interface unit (22). The memory directory interface unit (22) provides the invalidation request and identities of processors (16) affected by the invalidation request to the local block unit (28). The local block unit (28) determines which ones of the identified processors (16) are present in the computer system (10) and generates an invalidation message for each present processor (16) for transfer thereto. Each of the present processors (16) process their invalidation message and generate an acknowledgment message for transfer to the processor interface unit (24) that generated the invalidation request. The local block unit (28) determines which ones of the identified processors (16) are not present in the computer system (10) and generates an acknowledgment message for each non-existent processor (16). Each acknowledgment message is transferred to the processor interface unit (24) which generated the invalidation request.

15 Claims, 5 Drawing figures